



FORMAL

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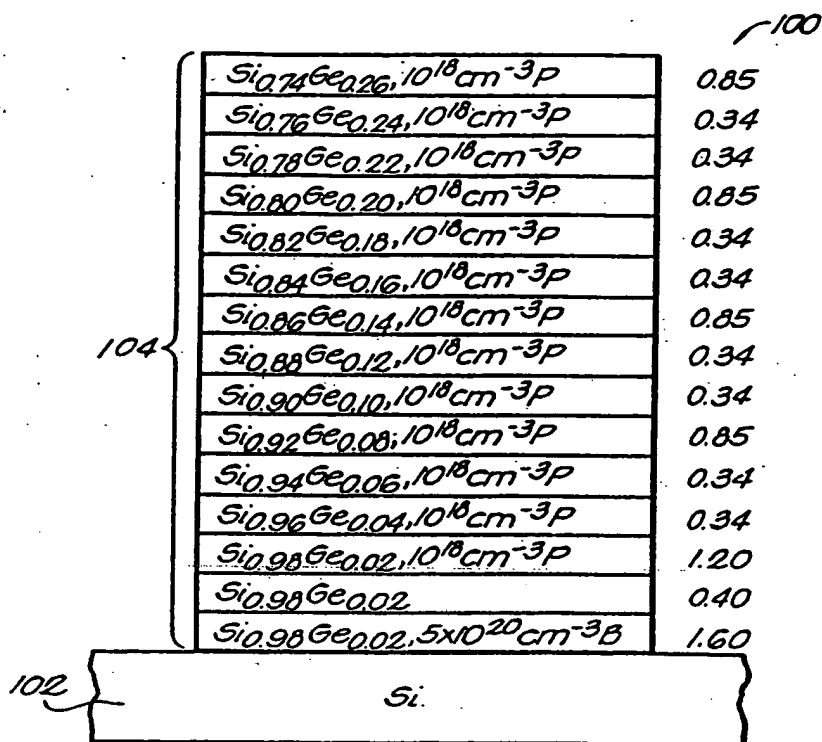


FIG. 1A

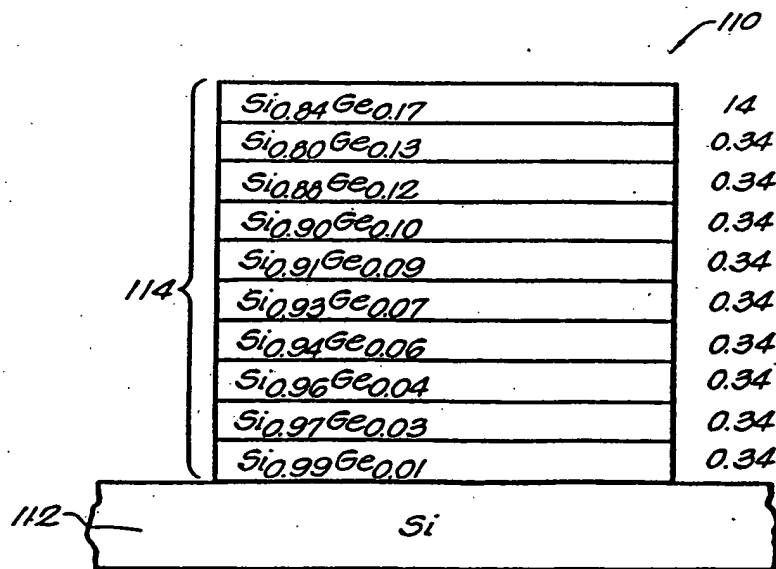


FIG. 1B

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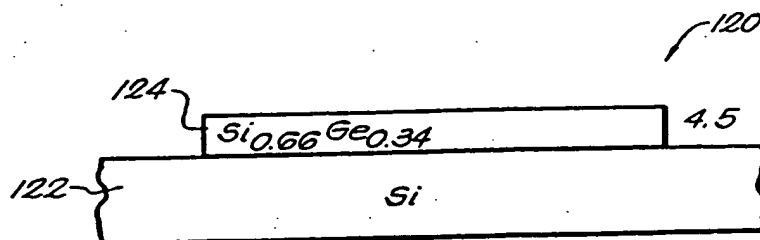


FIG. 1C

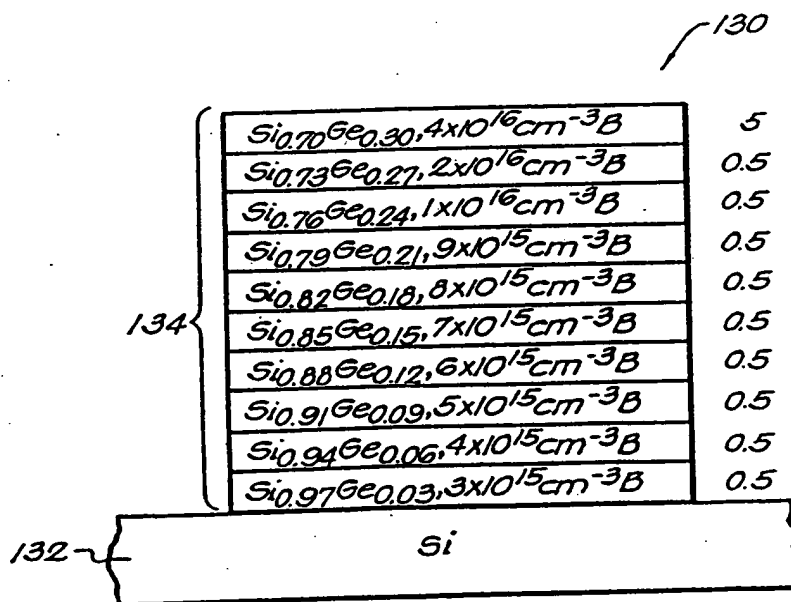
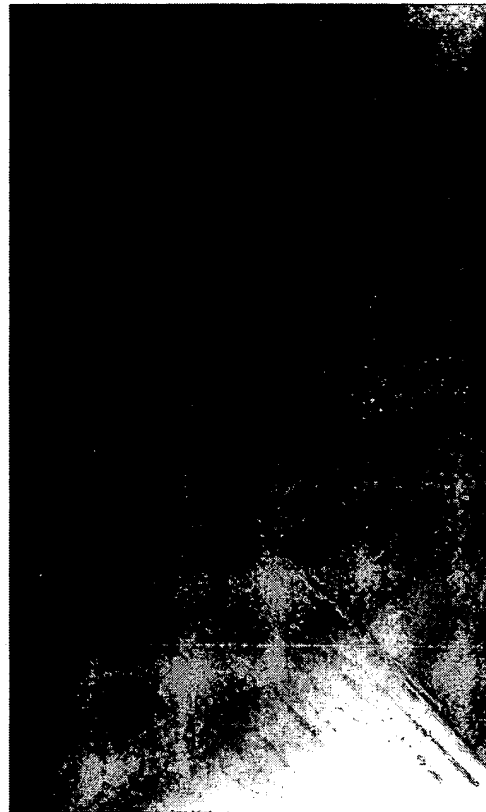


FIG. 1D

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FIG. 2



— 1.5 μm



THREADING
DISLOCATIONS

SILICON SUBSTRATE

FIG. 3

— 1.3 μm

FORMAL

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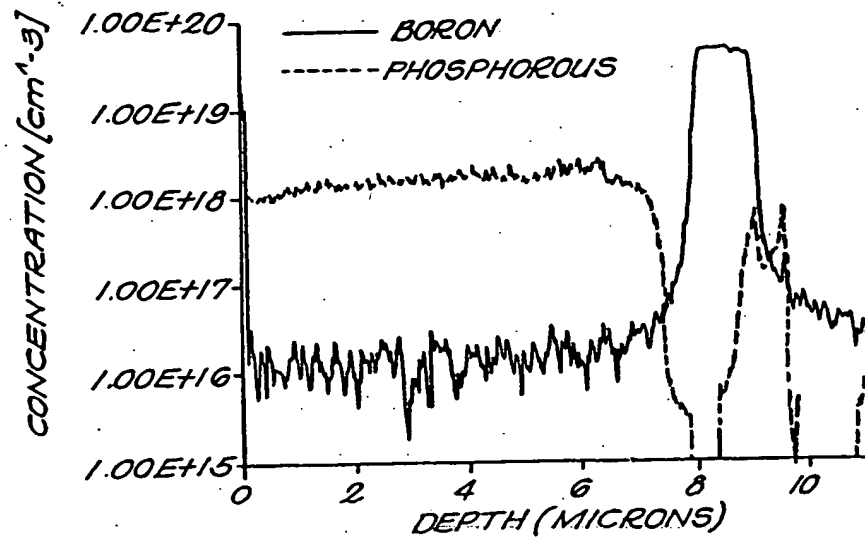


FIG. 4

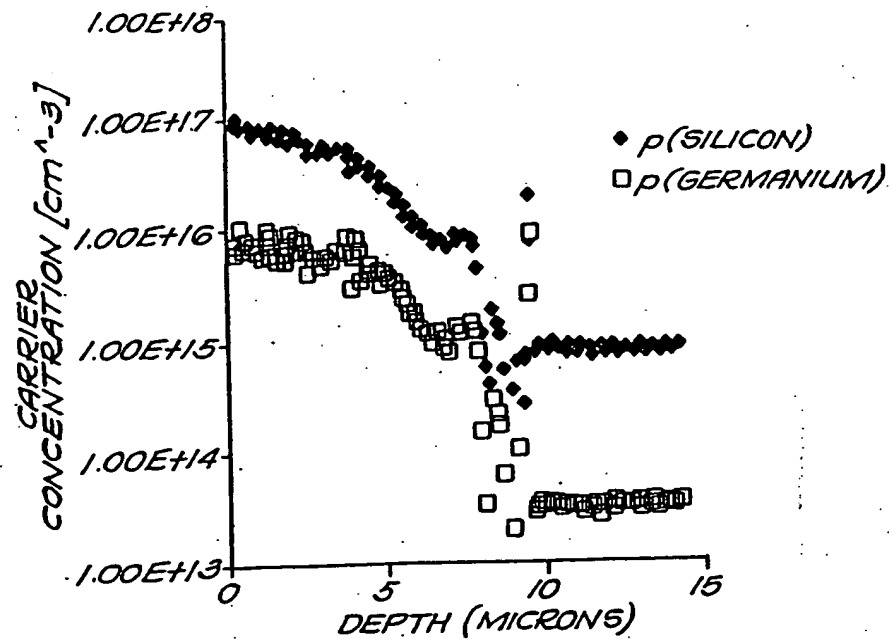


FIG. 5

FORMAL

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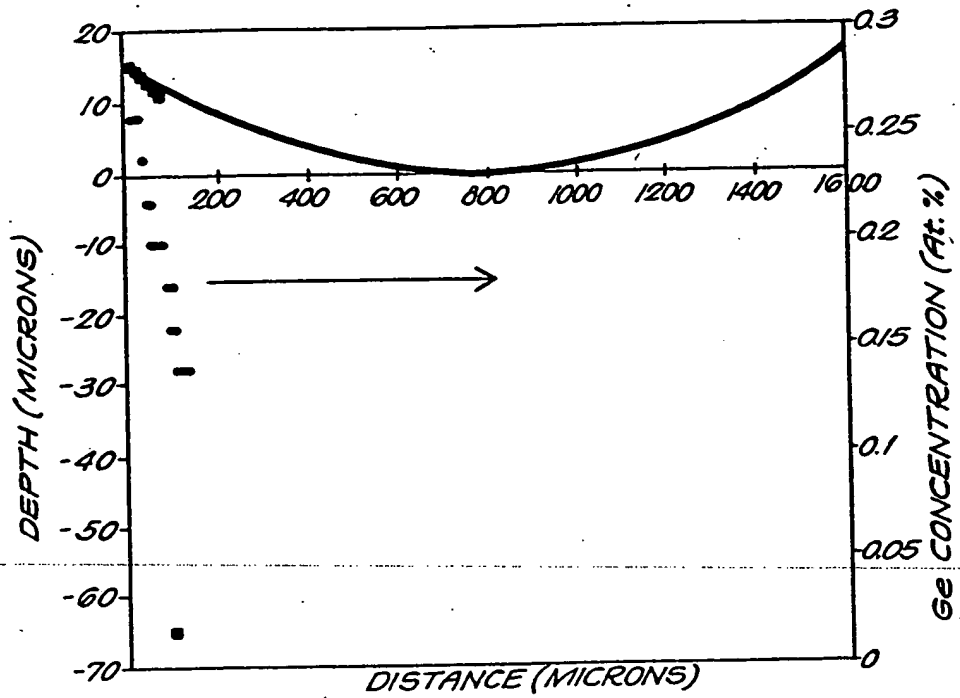


FIG. 6A

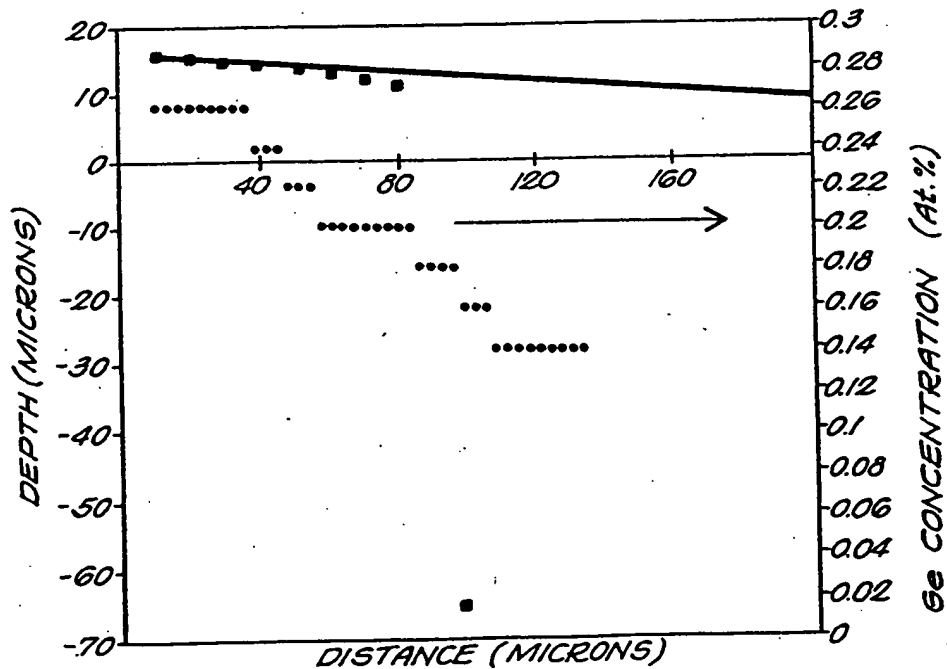


FIG. 6B

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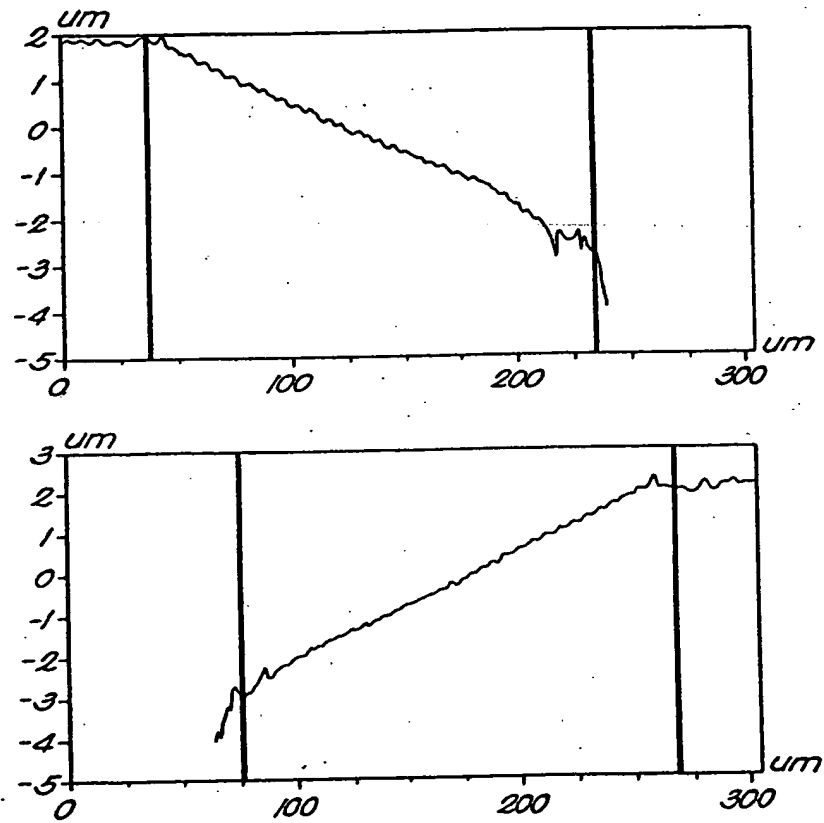


FIG. 7

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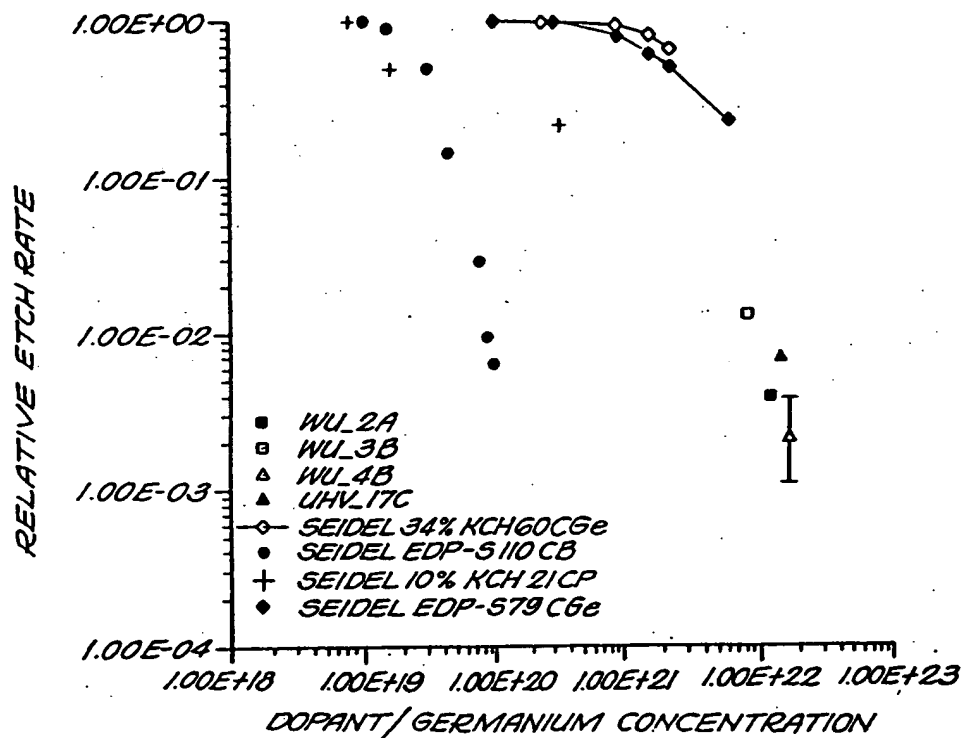


FIG. 8

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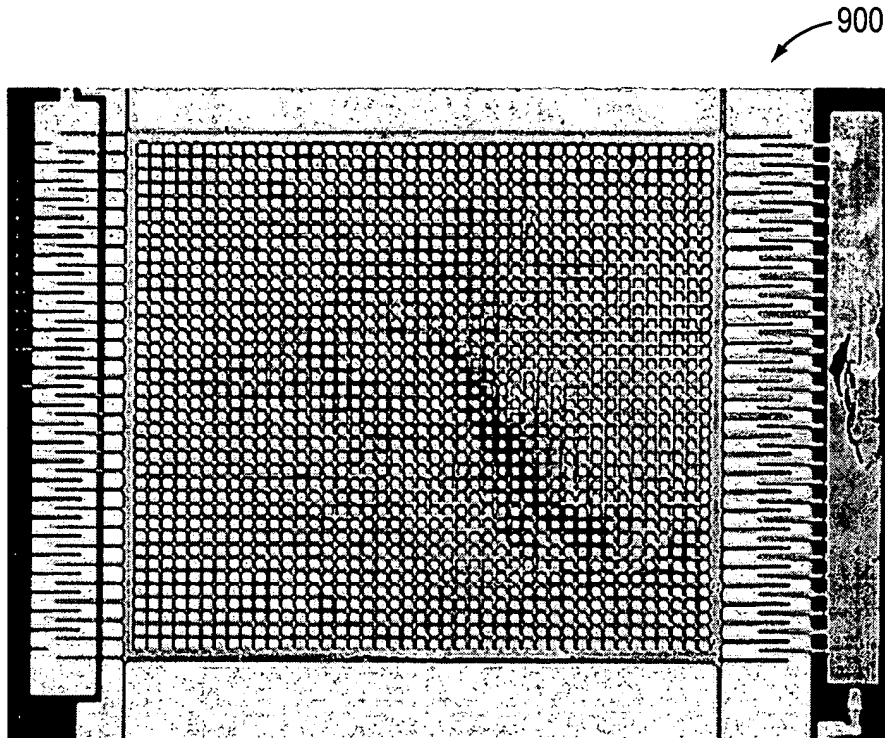


FIG. 9

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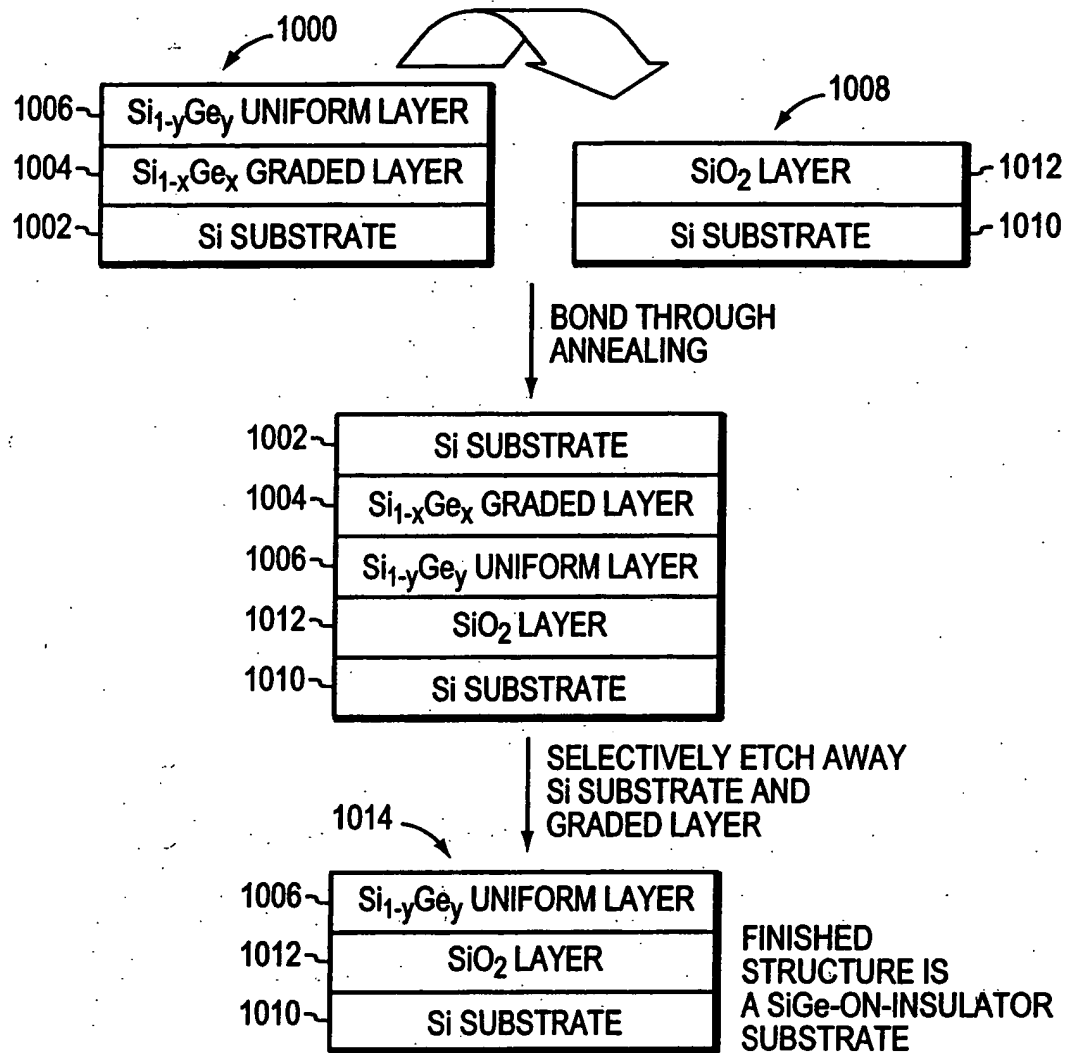


FIG. 10

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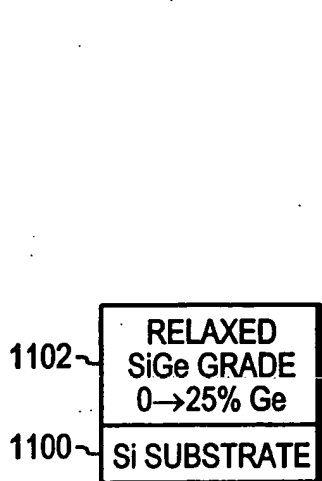


FIG. 11A

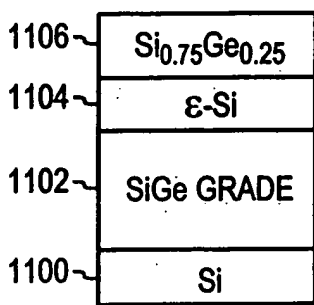


FIG. 11B

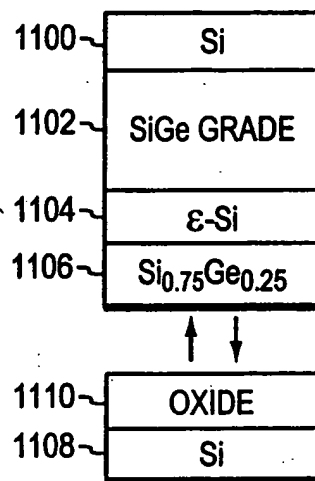


FIG. 11C

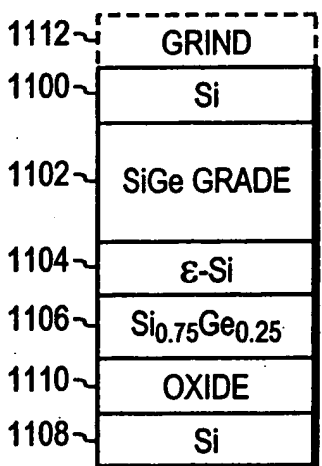


FIG. 11D

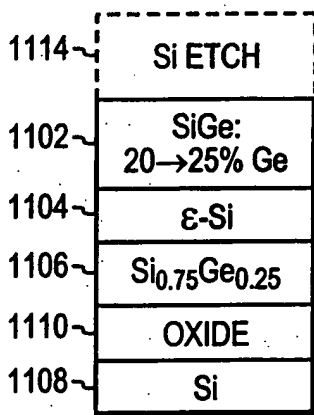


FIG. 11E

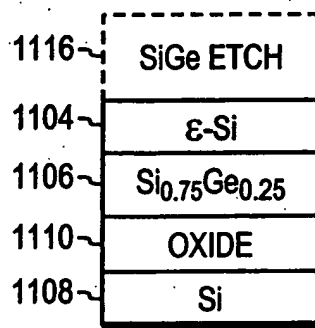


FIG. 11F

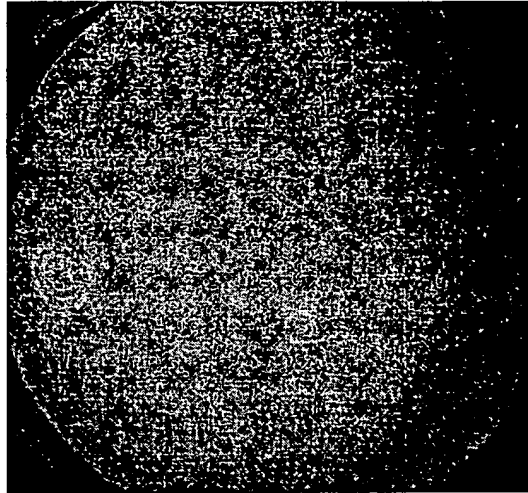


FIG. 12A

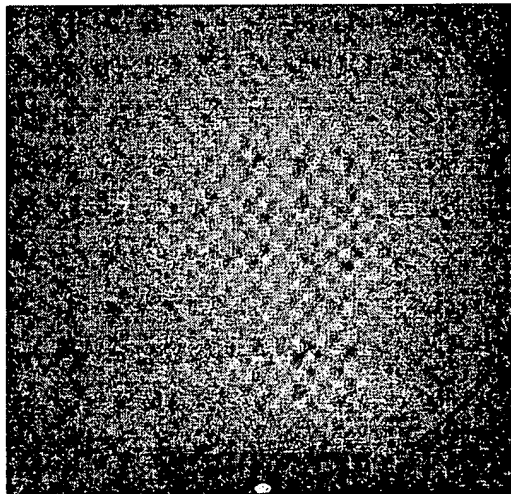


FIG. 12B

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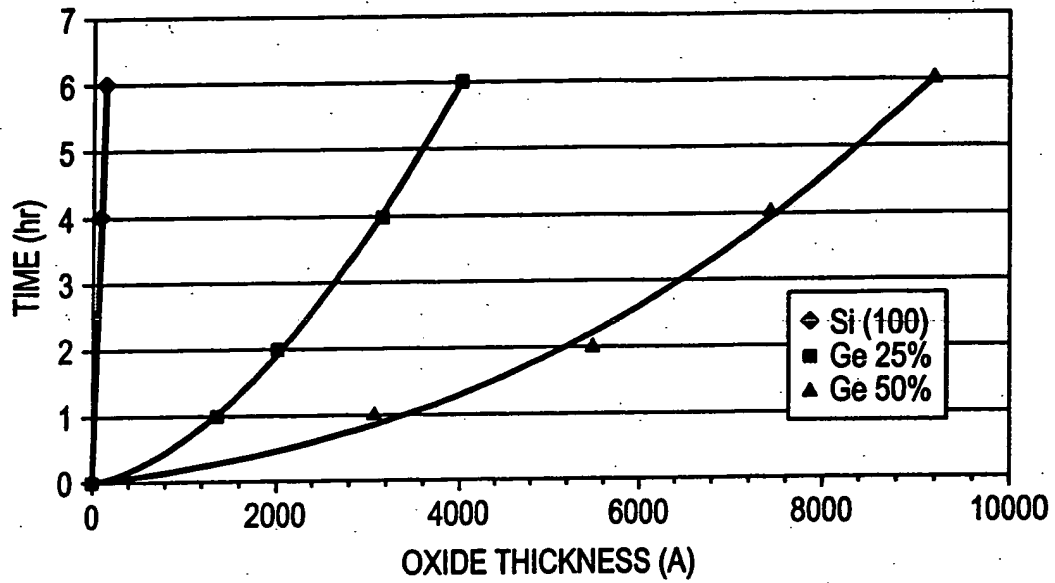


FIG. 13

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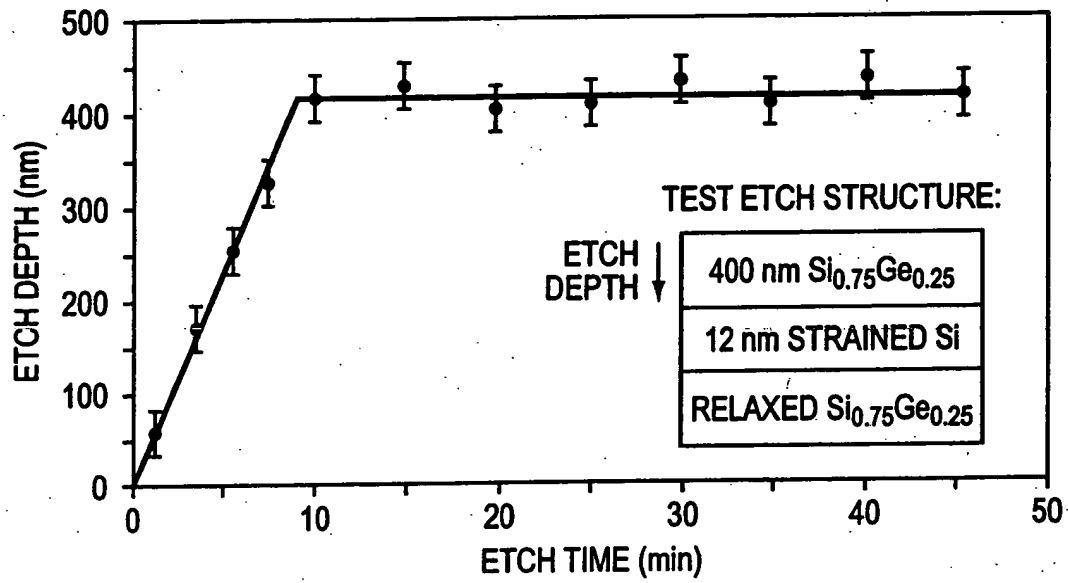


FIG. 14

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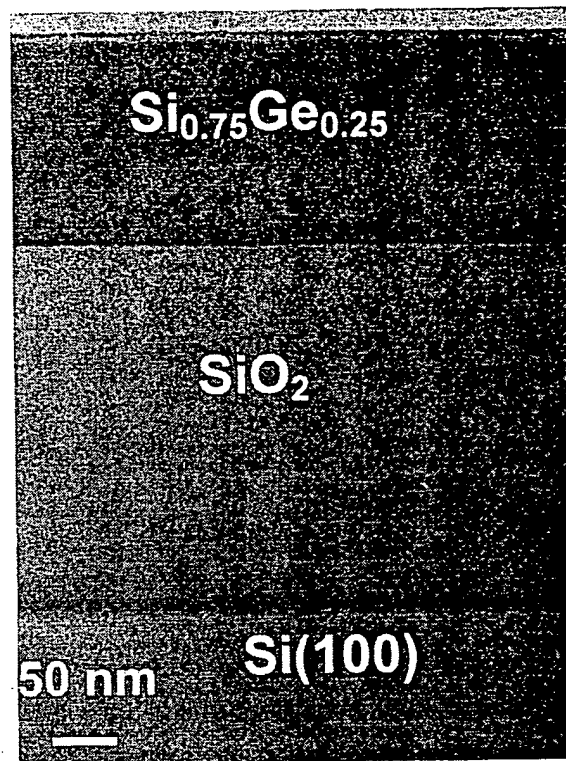


FIG. 15

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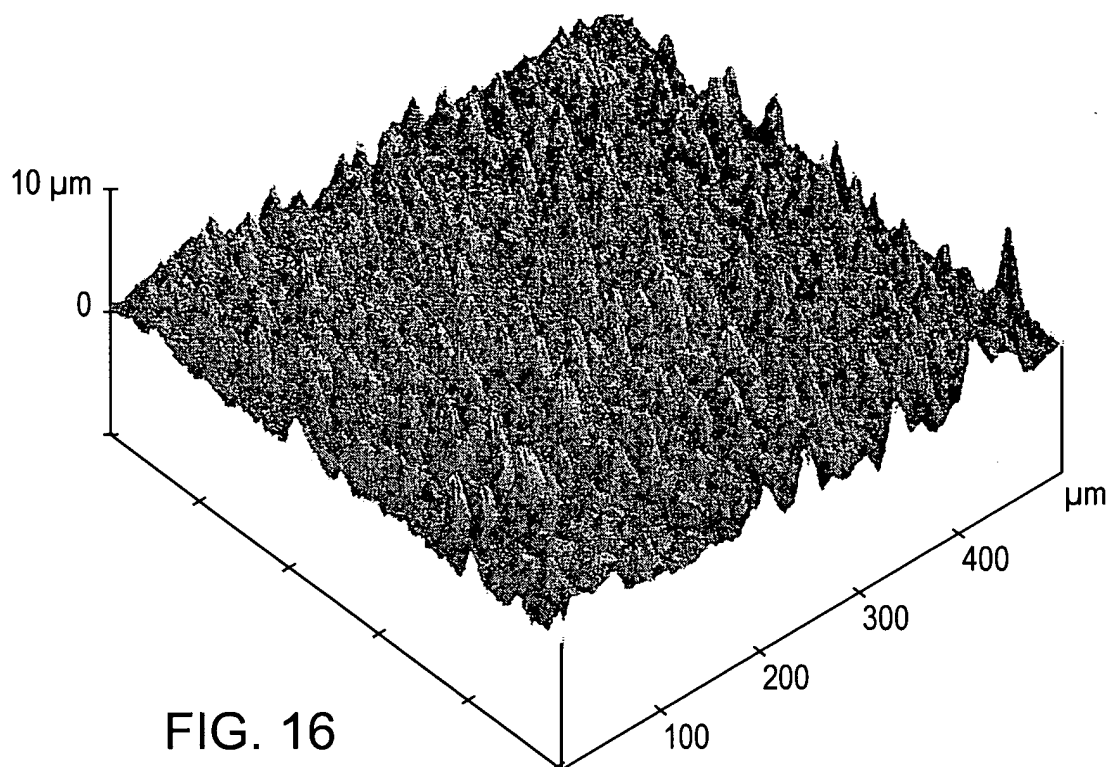


FIG. 16

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